



Universidad
de Alcalá

TEACHING GUIDE

Electronic Circuits Design for Communications

**Master in
Telecommunication Engineering**

Universidad de Alcalá

Academic Year 2021/2022

2nd Year - 1st Semester

TEACHING GUIDE

Course Name:	Electronic Circuits Design for Communications
Code:	201819
Master in:	Telecommunication Engineering
Department and area:	Electrónica Tecnología Electrónica
Type:	Compulsory
ECTS Credits:	6.0
Year and semester:	2nd Year, 1st Semester
Teachers:	Alfredo Gardel-Vicente Ignacio Bravo-Muñoz Álvaro Hernández-Alonso
Tutoring schedule:	Consultar al comienzo de la asignatura
Language:	Spanish / English Friendly

1. COURSE SUMMARY

The course Electronic Circuits Design for Communications aims to provide students knowledge on methodologies and tools for the design of HW/SW systems by using high-level languages. The general aim is that the student is capable to design, test and implement modules for an electronic communication system.

Assuming that students have previous backgrounds about the performance of a hardware system, programming a processor and simulation of communications algorithms, this course provides methodologies and techniques that allow them to implement high-performance systems in a short time and based on different available technological solutions.

The course has a strong practical component since theoretical explanations are supported by simulations and real implementations in configurable hardware systems. The development tools allow students to have a high degree of knowledge about the final resulting system. In the lab, designs are experimentally tested on a system-on-chip development board.

The online Virtual Classroom (Blackboard platform) will be used as a communication tool between teacher and student, and as repository for the different teaching materials and tasks. Students have to update Blackboard with a recent photograph and a valid email. This is essential for the realization of continuous assessment activities.

2. SKILLS

Basic, Generic and Cross Curricular Skills.

This course contributes to acquire the following generic skills, which are defined in the Section 3 of the Annex to the Orden CIN/355/2009:

en_CGT1 - Skill of analysis and synthesis.

en_CGT2 - Skill of organization and planning.

en_CGT3 - Skill to analyze and search for information from diverse sources

en_CGT4 - Skill to make decisions.

en_CGT5 - Skill to adapt to new situations.

en_CGT6 - Commitment to Human Rights, democratic principles, equality between women and men, solidarity, environmental protection and with the promotion of a culture of peace

en_CB6 - To have and understand knowledges that provide a basis or opportunity to be original in the development and/or application of ideas, often in a research context

en_CB7 - That students know how to apply the acquired knowledge and problem-solving abilities in new or unfamiliar environments within broader (or multidisciplinary) contexts related to their area of study.

en_CB8 - That students be able to integrate knowledge and face the complexity of making judgements based on incomplete or limited information that includes reflections on the social and ethical responsibilities linked to the application of their knowledge and judgements.

en_CB9 - That students be able to communicate their findings and the ultimate knowledge and reasons behind them to specialized and non-specialized audiences in a clear and unambiguous manner.

en_CB10 - That students have the learning skills that will enable them to continue studying in a

way that will be largely self-directed or autonomous.

en_CT1 - Troubleshooting skill

en_CT2 - Ethical commitment to work

en_CT3 - Skill to work in a team

en_CT4 - Working in a pressure environment

en_CT5 - Motivation for quality

Professional Skills

This course contributes to acquire the following professional skills, which are defined in the Section 5 of the Annex to the Orden CIN/355/2009:

en_CGestion1 - Ability to integrate technologies and systems typical of Telecommunications Engineering, with a generalist nature, and in broader and multidisciplinary contexts such as in bioengineering, photovoltaic conversion, nanotechnology, telemedicine.

en_CTecTel10 - Ability to design and manufacture integrated circuits

en_CTecTel11 - Knowledge of hardware description languages for highly complex circuits.

en_CTecTel12 - Ability to use programmable logic devices, as well as to design advanced electronic systems, either analog or digital.

en_CTecTel13 - Ability to design communications components, such as routers, switchers, transmitters and receiver in different bands

Learning Outcomes

After succeeding in this subject the students will be able to:

RA1. Carry out the design of whole projects, tests and refinement of advanced HW/SW electronic systems and equipment, for control and communications.

RA2. Design and implement electronic systems for communications by using pipelining techniques and selection of the arithmetic computing precision.

RA3. Knowledge and application of high-level languages for hardware description in programmable devices.

RA4. Ability to analyse and design circuits for clock signal generation/processing by means of oscillators/PLLs.

RA5. Ability to analyse HW/SW design methodologies in programmable electronic circuits for communications.

3. CONTENTS

Contents Blocks	Total number of hours
T1. Technologies, methodologies and tools for electronic design in communications. Primitives in the technological alternatives (programmable logic devices, FPGA). Review of HW systems design. Simulation, synthesis and implementation. Design of a HW system based on VHDL and IP Cores.	10 (6 lectures, 4 lab)
T2. Design of communication circuits. Electronic communication subsystems. Modules, oscillator, frequency synthesizers and NCOs. Circuits for modulation/demodulation – analog/digital. Design of a communication module – simulation and synthesis.	10 (4 lectures, 6 lab)
T3. Design of high-speed digital systems. Clock distribution and architecture pipelining. High-speed communications. Arithmetic circuits for digital signal processing. Numerical systems in electronic design for programmable logic devices.	16 (8 lectures, 8 lab)
T4. Hardware-Software co-design. Design and implementation of communications subsystems in configurable devices based on Systems-on-Chip (SoC).	18 (6 lectures, 12 lab)

4. TEACHING - LEARNING METHODOLOGIES. FORMATIVE ACTIVITIES.

4.1. Credits Distribution

Number of on-site hours:	60 hours
Number of hours of student work:	90
Total hours	150

4.2. Methodological strategies, teaching materials and resources

The teaching-learning process will be carried out through the following activities:

- Descriptive lectures in large groups that allow the teacher to introduce the required contents for the correct development of the learning process. These lectures will present essential contents later serving to develop broader skills. Additionally, the students' active participation in the proposed activities will be required.
- Laboratory practical sessions. Different practices will be developed in a coordinated way, involving the theoretical concepts, so students can experimentally verified the knowledge previously acquired, either individually or in group.

Throughout the course, theoretical and practical activities and tasks will be proposed for students. Practices will be developed in a coordinated way with the theoretical lectures. For the practical sessions, students will have available a laboratory post with basic equipment (oscilloscope, power supply, function generator), the necessary experimental set-up for tests, as well and the suitable design and simulation software in a computer. The lab practices will be carried out in groups no larger than two people.

Furthermore, the following complementary resources can be used

- Individually or in group works: they could imply, together with the corresponding study and development, a public presentation for the rest of students in the group for further discussion.
- Attending scientific conferences, meetings or discussions related to the contents.

Throughout the learning process in this course, students must use different bibliographical or electronic sources and resources, so they become familiar with documentation that they will use professionally in the future. In addition, lecturers will provide materials necessary to follow the course (theoretical principles, exercises and problems, practical manuals, audio-visual references, etc.), so that students can fulfil the objectives of the course and achieve the proposed skills.

Students may attend group or individual tutorials (if requested by students). These tutorials will allow any question to be solved and to consolidate the acquired knowledge. They will help to properly monitor students and to assess the adequate progress of the teaching-learning process.

5. ASSESSMENT: procedures, evaluation and grading criteria

Preferably, students will be offered a continuous assessment model that has characteristics of formative assessment in a way that serves as feedback in the teaching-learning process.

5.1. PROCEDURES

The evaluation must be inspired by the criteria of continuous evaluation (Learning Assessment Guidelines, LAG, art 3). However, in compliance with the regulations of the University of Alcalá, an alternative process of final evaluation is made available to the student in accordance with the [Learning Assessment Guidelines](#) (last modified in the Governing Board of October 31, 2019) as indicated in Article 10, students will have a period of fifteen days from the start of the course to request in writing to the Director of the Polytechnic School their intention to take the non-continuous evaluation model adducing the reasons that they deem convenient. The evaluation of the learning process of all students who do not apply for it or are denied it will be done, by default, according to the continuous assessment model. The student has two calls to pass the subject, one ordinary and one extraordinary.

Ordinary Call

Continuous Assessment:

it consists in following the course by means of the proposed activities to be carried out before lectures and lab sessions, by means of the lecture questions or forums in virtual platforms. The performance in the lab practices and the intermediate and final tests will be also considered. Deliveries will be organized throughout the semester.

Assessment through final exam:

In the case of evaluation by means of a final exam, the evaluation elements to be used will be successfully passing two lab practices, a course work and the final assessment test.

Extraordinary Call

It will consist in a final assessment test, together with new lab practices to be developed by students in order to improve final marks.

5.2. EVALUATION

EVALUATION CRITERIA

The assessment criteria measure the level in which the competences have been acquired by the student. For that purpose, the following are defined::

CE1. Students know the technological alternatives, methodologies and tools necessary to carry out a hardware/software electronic design.

CE2. Students have acquired technical knowledge about high-speed digital systems, arithmetic circuits and pipelined process

CE3. Students have acquired technical knowledge about high-level language for hardware/software circuit description

CE4. Students are able to solve practical problems associated to electronic circuits design for communications

CE5. Students can design an electronic system by HW/SW co-design on Systems-on-Chip based on configurable devices

GRADING TOOLS

The work of the student is graded in terms of the assessment criteria above, through the following tools:

1. Continuous assessment (CA) about the course following by means of the required critical exercises for some readings and video conferences, as well as students' participation in lectures and in virtual forums.
2. Deliveries of lab practices (D1 to D3):
 - 2.1. In delivery D1 students must design a signal generation system on configurable hardware as a review and updating of the necessary background. Students must test modules used in communication circuits managing clock signals, data communications, and system synchronization.
 - 2.2. In delivery D2 students must design arithmetic circuits described in high-level language.
 - 2.3. In delivery D3 students must solve practical aspects of a SoC implementation on a development platform.
3. Final exam (FE): it is based on practical problems about the design and synthesis of electronic circuits, as well as on theoretical questions about the course contents.

GRADING CRITERIA

In the ordinary call-continuous assessment the relationship between the competences, learning outcomes, criteria and evaluation instruments is as follows.

Skill	Learning Outcomes	Evaluation criteria	Grading Tool	Contribution to the final mark
CB6-10, CGT1-6, CT1-5, CTecTel10-13	RA1, RA4	CE1, CE4	CA, D1	25%
CB6-10, CGT1-6, CT1-5, CTecTel10-13	RA2, RA3	CE2, CE3, CE4	CA, D2	25%
CB6-10, CGT1-6, CT1-5, CGestion1, CTecTel10-13	RA3, RA5	CE1, CE5	CA, D3	25%
CB7, CGT1, CTecTel11-13	RA1, RA2, RA3, RA4	CE1, CE2, CE3	FE	25%

In the ordinary call **final evaluation**, the relationship between the competences, learning outcomes, criteria and evaluation instruments is as follows.

Skill	Learning Outcomes	Evaluation criteria	Grading Tool	Contribution to the final mark
CB6-10, CGT1-6, CT1-5, CTecTel10-13	RA1, RA4	CE1, CE4	D1	25%
CB6-10, CGT1-6, CT1-5, CTecTel10-13	RA2, RA3	CE2, CE3, CE4	D2	25%
CB6-10, CGT1-6, CT1-5, CGestion1, CTecTel10-13	RA3, RA5	CE1, CE5	D3	25%
CB7, CGT1, CTecTel11-13	RA1, RA2, RA3, RA4	CE1, CE2, CE3	FE	25%

Extraordinary call

In the case of the extraordinary call, the same percentages that have been established in the case of the evaluation by means of a final exam will be maintained, giving the option of making the Dx practices or maintaining the mark obtained in the CA (continuous assesment) or in the FE (final evaluation), according to the student's decision. In any case, the Dx will be made by those students who have not done it in the final exam option in the ordinary call.

6. BIBLIOGRAPHY

6.1. Basic Bibliography

- Documents prepared by lecturers, provided to students, or published in the course website.
- Website about the contents involved in the course, previously oriented by lecturers.
- [Beasley, 2008] "Modern Electronic Communication (9th Edition)", Jeffrey S. Beasley, Gary M. Miller. Pearson, 2008
- [Churiwala, 2017] "Designing with Xilinx® FPGAs Using Vivado". Churiwala, Sanjay. Springer, 2017.
- [Deschamps , 2006] "Synthesis of arithmetic circuits: FPGA, ASIC and embedded systems", J.P. Deschamps, G.J.A. Bioul, G.D. Sutter, John Wiley & Sons 2006• [Faundez, 2004] "Circuitos Electrónicos para Sistemas de Comunicaciones", Marcos Faundez Zanuy , 2004. Ediciones Ceysa.
- [Flynn , 2011] "Computer System Design: System-on-Chip", Michael J. Flynn, Wayne Luk, Wiley 2011
- [Julián, 2015] "Circuitos Integrados Digitales CMOS: Análisis Y Diseño". Pedro Julián. Marcombo (2015)
- [Meyer-Baese, 2007] "Digital Signal Processing with Field Programmable Gate Arrays (Signals and Communication Technology)". Uwe Meyer-Baese, Third Edition, Springer 2007.
- [Sass ,2010] "Embedded Systems Design with Platform FPGAs: Principles and Practices. 2010". Ronald Sass, Andrew G. Schmidt. Morgan Kauffman, 2010.
- [Schaumont, 2012] "A Practical Introduction to Hardware/Software Codesign (2nd ed)". Patrick Schaumont. Springer, 2012

- [Stauffer, 2008] “High Speed Serdes Devices and Applications”. D.R. Stauffer, J. Trinko, M.A. Sorna, K. Dramstad, C. Rosser, A. Mohammad, J. Donald. Springer, 2008.

6.2. Additional Bibliography

- [Gary, 2009] “Analysis and design of analog integrated circuits”, Paul R. Gary, Paul J. Hust, Stephen H. Lewis , Tobert G. Meyer, Wiley. 2009
- [Hennesy, 2012] “Computer Architecture: A Quantitative Approach”. John L. Hennesy y David A. Patterson, 5th edition, Morgan Kaufmann, 2012.
- [Hübner, 2011] “Multiprocessor system-on-chip hardware design and tool integration”, Michael Hübner, Springer, 2011
- [Noergaard. 2013] “Embedded Systems Architecture: A Comprehensive Guide for Engineers and Programmers”. Tammy Noergaard., 2nd edition, Newnes, 2013
- [Sicard, 2007] “Advanced CMOS Cell Design”. E. Sicard, S. D. Bendhia. McGraw-Hill. 2007

Disclosure Note

The University of Alcalá guarantees to its students that, if due to health requirements the competent authorities do not allow the total or partial attendance of the teaching activities, the teaching plans will achieve their objectives through a teaching-learning and evaluation methodology in online format, which will return to the face-to-face mode as soon as these impediments cease.